

interconnection conductors to one another and to said plurality of logic resources, said programmable

10 interconnection resources being less than fully populated; said programmable logic device further comprising:

at least one random access memory having a read port and a write port;

15 a first programmable interconnection resource in said plurality of programmable interconnection resources for connecting port conductors in said read port to a selected one of said plurality of groups of interconnection conductors; and

20 a second programmable interconnection resource in said plurality of programmable interconnection resources for connecting port conductors in said write port to said selected one of said plurality of groups of interconnection conductors; wherein:

25 said read port has a first number of read port conductors;

said write port has a second number of write port conductors;

30 said first number is equal to said second number, each read port conductor in said read port having a corresponding write port conductor in said write port; and

35 said first and second programmable interconnection resources are populated to allow connection of each individual conductor in said selected one of said plurality of groups of interconnection conductors to an individual read port conductor in said read port and to an individual write port conductor, corresponding to said individual read port conductor, in said write port.

3. (amended) A digital processing system comprising:

5 processing circuitry;
a system memory coupled to said processing circuitry; and

coupled to the processing circuitry and the
system memory, a programmable logic device comprising:
a plurality of logic resources,
a plurality of groups of interconnection
10 conductors for interconnecting said logic resources, and
a plurality of programmable interconnection
resources for connecting conductors in said groups of
interconnection conductors to one another and to said
plurality of logic resources, said programmable
15 interconnection resources being less than fully populated,
said programmable logic device further comprising:
at least one random access memory having a
read port and a write port,
a first programmable interconnection resource
20 in said plurality of programmable interconnection resources
for connecting port conductors in said read port to a
selected one of said plurality of groups of interconnection
conductors, and
a second programmable interconnection
25 resource in said plurality of programmable interconnection
resources for connecting port conductors in said write port
to said selected one of said plurality of groups of
interconnection conductors, wherein:
said first and second programmable
30 interconnection resources are populated to allow connection
of an individual conductor in said selected one of said
plurality of groups of interconnection conductors to
corresponding port conductors in both said read port and
said write port.

4. (amended) A printed circuit board on which is
mounted a programmable logic device, said programmable logic
device comprising:

a plurality of logic resources;
5 a plurality of groups of interconnection
conductors for interconnecting said logic resources; and

10 a plurality of programmable interconnection
resources for connecting conductors in said groups of
interconnection conductors to one another and to said
plurality of logic resources, said programmable
interconnection resources being less than fully populated;
said programmable logic device further comprising:

at least one random access memory having a
read port and a write port;

15 a first programmable interconnection resource
in said plurality of programmable interconnection resources
for connecting port conductors in said read port to a
selected one of said plurality of groups of interconnection
conductors; and

20 a second programmable interconnection
resource in said plurality of programmable interconnection
resources for connecting port conductors in said write port
to said selected one of said plurality of groups of
interconnection conductors; wherein:

25 said first and second programmable
interconnection resources are populated to allow connection
of an individual conductor in said selected one of said
plurality of groups of interconnection conductors to
corresponding port conductors in both said read port and
30 said write port.

7. (amended) An integrated circuit comprising:

3
5 a plurality of semiconductor devices;
a plurality of groups of interconnection
conductors for interconnecting said semiconductor devices;
and

a plurality of programmable interconnection
resources for connecting conductors in said groups of
interconnection conductors to one another and to said
plurality of semiconductor devices, said programmable
10 interconnection resources being less than fully populated;
said integrated circuit further comprising:

at least one random access memory having a
read port and a write port;

15 a first programmable interconnection resource
in said plurality of programmable interconnection resources
for connecting port conductors in said read port to
conductors in a selected one of said plurality of groups of
interconnection conductors; and

20 a second programmable interconnection
resource in said plurality of programmable interconnection
resources for connecting port conductors in said write port
to conductors in said selected one of said plurality of
groups of interconnection conductors; wherein:

25 said read port has a first number of read
port conductors;

said write port has a second number of write
port conductors;

30 said first number is equal to said second
number, each read port conductor in said read port having a
corresponding write port conductor in said write port; and

said first and second programmable
interconnection resources are populated to allow connection
of each individual conductor in said selected one of said
plurality of groups of interconnection conductors to an
35 individual read port conductor in said read port and to an
individual write port conductor, corresponding to said
individual read port conductor, in said write port.

9. (amended) A digital processing system
comprising:

5 processing circuitry;
a system memory coupled to said processing
circuitry; and
coupled to the processing circuitry and the
system memory, an integrated circuit comprising:
a plurality of semiconductor devices,

10 a plurality of groups of interconnection
conductors for interconnecting said semiconductor devices,
and

a plurality of programmable interconnection
resources for connecting conductors in said groups of
interconnection conductors to one another and to said
15 plurality of semiconductor devices, said programmable
interconnection resources being less than fully populated,
said integrated circuit further comprising:

at least one random access memory having a
read port and a write port,

20 a first programmable interconnection resource
in said plurality of programmable interconnection resources
for connecting port conductors in said read port to
conductors in a selected one of said plurality of groups of
interconnection conductors, and

25 a second programmable interconnection
resource in said plurality of programmable interconnection
resources for connecting port conductors in said write port
to conductors in said selected one of said plurality of
groups of interconnection conductors, wherein:

30 said first and second programmable
interconnection resources are populated to allow connection
of an individual conductor in said selected one of said
plurality of groups of interconnection conductors to
corresponding port conductors in both said read port and
35 said write port.

10. (amended) A printed circuit board on which is
mounted an integrated circuit, said integrated circuit
comprising:

5 a plurality of semiconductor devices;
a plurality of groups of interconnection
conductors for interconnecting said semiconductor devices;
and

a plurality of programmable interconnection
resources for connecting conductors in said groups of